

M2192 SERIES

DC/DC POWER SUPPLY



PRODUCT HIGHLIGHTS

- VITA 62 1" Pitch
- SOSA™ ALIGNED
- 3U FORM FACTOR
- 600W Steady State
- NED (Optional)
- OPERATING TEMP: -55°C to +85°C
- EMI: Compliant to MIL-STD-461G (5μ LISN)
- Environmental: MIL-STD-810
- :Input Options
 - MIL-STD-704
 - Mil-STD-1275

SPECIAL FEATURES

- VITA 62 Compliant
- Aligned with the SOSA™ Technical Standard
- Wide input range
- Up to 600W output Steady state power
- Supports Mil-STD-1275E
- NED¹
- Remote sense
- Current Sharing²
- Fixed switching frequency (220 kHz)
- Indefinite short circuit Protection
- Reverse battery protection
- Over temperature shutdown with auto-recovery
- EMI filters included
- System Management: protocol per VITA 46.11
 - Output voltages and currents
 - Card temperature
 - Card system status

¹ Optional by PN. Please see NED section for full compliance

² Optional by PN

Electrical Specifications

DC Input

18 to 48V_{DC} steady state
 30Sec Turn-off timer when input voltage goes below 20V
 Works through MIL-STD-1275E (Surges: 12V Initial Engagement, 16V Cranking, 100V)

DC Output

PO1 & PO3 (VS1): 12V up to 50A
 PO2 (3.3VAux): 3.3V up to 15A

Isolation

Over 20 MΩ at test voltage:
 200V between Input and Output
 200V between Input and Case
 100V between Output and Case

Current Sharing

12V A.C.S
 3.3VAux P.C.S (A.C.S optional)

EMC

Design to meet:
 MIL-STD-461G¹
 CE101, CE102, CS101,
 CS114, CS115, CS116

Efficiency

Up to 87 %

Notes:

1. Compliance achieved with 5μH LISN and static resistive load.

Line/Load regulation

Ripple and Noise

Typically, less than 50mV_{p-p} (max. 1%_p). Measured across a 0.1μF capacitor and 10μF capacitor on load at Input Voltage of 18V-36V, all Temperature Range.

Normal Quiescent Current:

Inhibited Output: 193mA (3.3VAux Only)
 Disabled Input: 112mA (All Outputs Off)

System management options:

- 1) I2C
- 2) Custom IPMI
- 3) VITA 46.11 Tier II IPMC

Data available:

- Output voltages and currents
- Input voltage
- Card
- temperature

Load Transient Overshoot and Undershoot

Output dynamic response of less than 5% at load Step of 30%-60%.
 Output returns to regulation in less than 1mSec

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Environmental ¹

Design to Meet MIL-STD-810G

Temperature

Operating: -55°C to +85°C at unit Edge

Storage: -55°C to +125°C Designed

Design to meet 600 cycles VITA47

Altitude

Method 500.5, Procedure I & II

Storage/Air transport 40Kft

Operation/Air carriage 70Kft

Salt Fog

Method 509.5

Fungus

Does not support fungus growth, in accordance with the guidelines of

Mil-STD-454, Requirement 4.

Humidity

Method 5007.5, Up to 95% RH

Vibration & Shock

Shock: Saw tooth- 40h, 11mSec

Vibration: Vita47 ClassV3.

Reliability: TBD Hours, calculated IAW MIL-HDBK-217F Notice 2 at +65 °C, GF.

Note 1: **Environmental Stress Screening (ESS)** Including random vibration and thermal cycles is also available. **.Please consult factory for details**

Protections ¹

Input

- **Inrush Current Limiter**

Peak value of $5 \times I_{IN}$ for initial inrush currents lasting more than 50 μ Sec.

- **Under Voltage**

Unit shuts down when input steady state voltage drops below $17 \pm 0.5V_{DC}$.

Automatic restart when input voltage returns to nominal range.

- **Input Overvoltage Protection**

shuts down when input steady state voltage rise above $55/85 \pm 2V_{DC}$. Automatic restart when input voltage returns to nominal range.

Output

- **Passive over voltage**

protection on 3.3VAux
3.9V Zener.

- **Active over voltage**

protection on 12V output
20% \pm 5% above nominal voltage.
Automatic recovery when output voltage drops below threshold.

- **Overload / Short-Circuit protection**

Continuous protection (10-30% above maximum current) for U_{Unit} unlimited time (Hiccup). steady state Automatic recovery when overload/short circuit removed.

General

- **Over Temperature Protection**

Automatic shutdown at internal temperature of $95 \pm 5^\circ C$. Automatic recovery when temperature drops below $90 \pm 5^\circ C$.

Note 1: Thresholds and protections can be modified / removed (please consult factory)

Functions and Signals - According to VITA 62

Signal Name	Type	Description
*FAIL	Output	Indicates to other modules in the system that a failure has occurred in one of the outputs. Please refer to Figure 2 ¹
*SYSRESET	Output	Indicates to other modules in the system that all outputs are within their working level. Please refer to Figure 2 ¹
*INHIBIT	Input	Controls power supply outputs. This signal in conjunction with ENABLE controls the outputs. Please refer to Table 1 and Figure 1 ¹
*ENABLE	Input	Controls power supply outputs. This signal in conjunction with INHIBIT controls the outputs. Please refer to Table 1 and Figure 1 ¹
NED	Output	NED event detector output. Normally Low, goes high and Latch during Event. Internal 2K pullup to 3.3V
NED RETURN	Output	NED Return ¹
GA0, GA1*, GA2	Input	Used for geographical addressing. GA2 is the most significant bit and GA0 is the least significant bit. ¹
SCL_A, SDA_A	Bidirectional	I2C bus Clock and Data respectively. Through this bus the voltage and temperature readouts can be shared. ¹
SCL_B, SDA_B	Bidirectional	Redundant I2C bus Clock and Data respectively. Through this bus the voltage and temperature readouts can be shared. ¹
Sync_In	Input	TBD.
VOUT SENSE	Input	The SENSE is used to achieve accurate load regulations at load terminals (this is done by connecting the pins directly to the load's terminals).
3.3Vaux A.C.S	Bidirectional	Support 3.3Vaux Active current share between Outputs. See Current Share para. ^{1 2 3} (Optional, non-SOSA configuration)
PO#_SHARE	Bidirectional	Support current share between Outputs ¹

:Notes

1. Signal referenced to **SIGNAL RTN**.
2. When not used leave open
3. for 3.3Vaux In Passive or Non-Current Share configuration, this pin is Internally Disconnected.

Table 1 – Inhibit and Enable Functionality

*INHIBIT	Low	Low	High	High
*ENABLE	Low	High	Low	High
VS1	OFF	OFF	ON	OFF
3.3V	ON	OFF	ON	OFF

Figure 1 – Inhibit and Enable Input stage

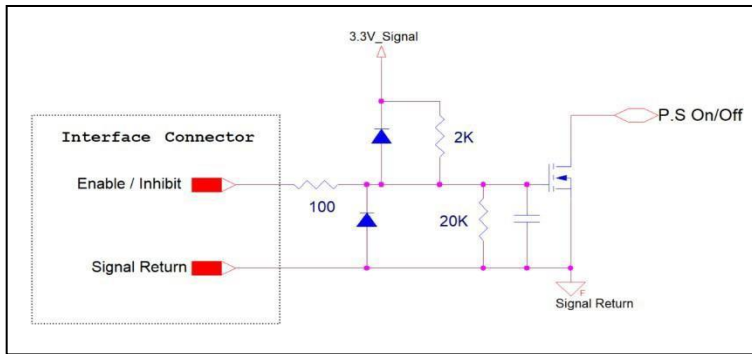


Figure 2 – SysRst and Fail bit Output Stage

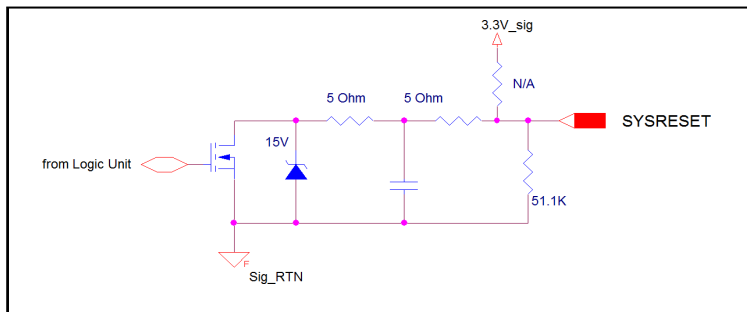
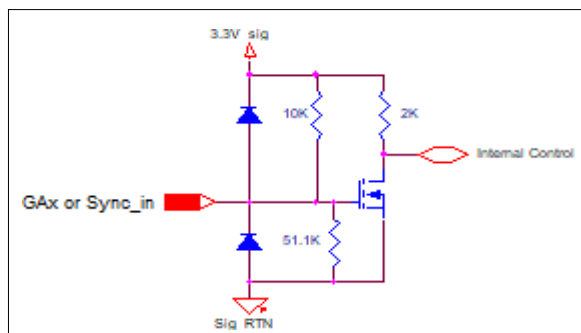
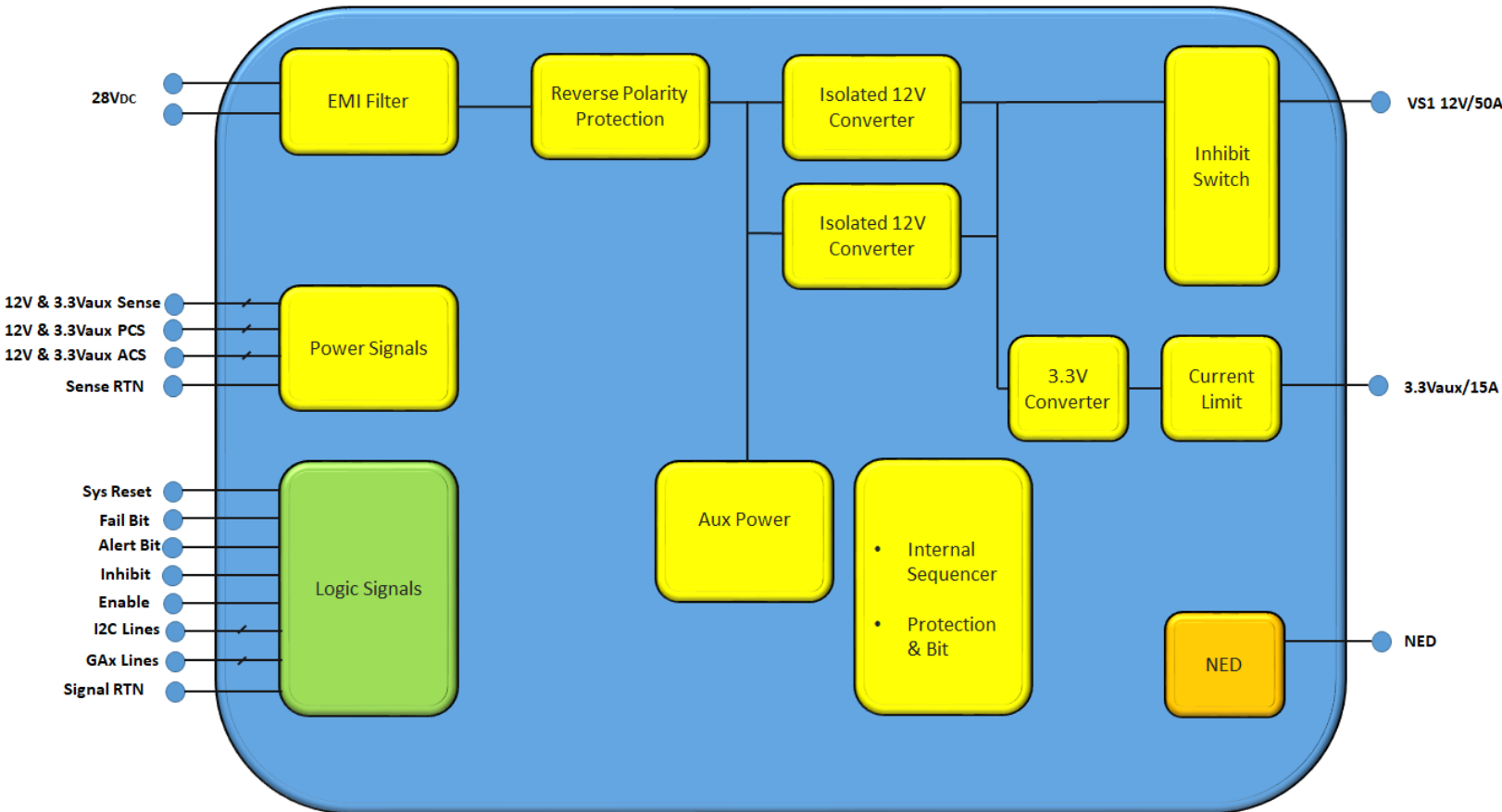


Figure 3 – GAx and Sync_In Stage



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Simplified Block Diagram



Detailed Information

1. M2192 Input Voltage Operatin

The M2192 steady state operation voltage is 18V to 48V and will continuously work through Mil-STD-1275E. 12V and 100V Surges

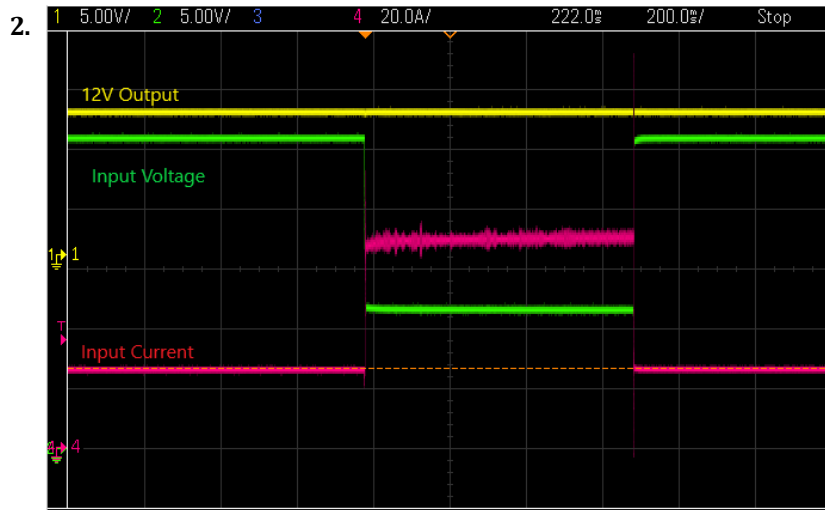
1.1 Steady state Low Line Turn-on and Turn-off Limits

To avoid Turn-on and Turn-off glitch the unit have about 2V Hysteresis. The Turn-on threshold is under 20V and turn- off under 18V.

Those limits can be adjusted, contact Factory for more information.

Unit will automatically shut down after about 30Sec if input voltage remains under 20V.

1.2 Mil-STD-1275E, 12V Input Transient



3. Outputs Voltage Regulation

The M2192 contains accurate internal sense lines to keep output voltage at less than 4% regulation for all Line/ Load and temperature range (see Table 2).

Output Voltage Range	/12V50A	3.3V/15A
Active Current Share	11.85V - 12.15V	3.28V - 3.42V
Passive Current Share	N/A	3.25V - 3.45V

Table 2: Outputs voltage regulation. VIN 18V to 48V, Temperature -55 to 85 °C

3.1 Sense Lines

Sense Lines are provided for 12V and 3.3V outputs to compensate line voltage drop. *Sense Lines* proper connection is shown in Figure 3.

Each VSx output has its own *Sense Lines*, additional common *Sense RTN Line* is provided for all VSx Outputs (VITA 62 Standard).

Contact Factory for Sense configuration different than the VITA 62 standard

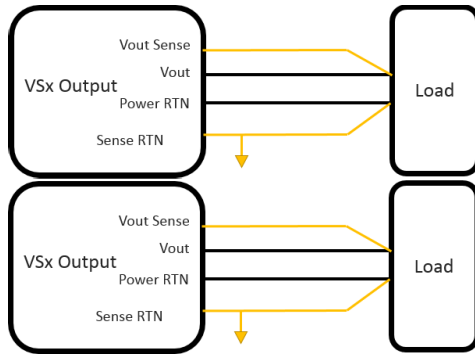


Figure 4: M2192 Sense line connection

4. Current Share (C.S)

Current Share of two or more units is optional (Contact Factory)
 12V output and 3.3Vaux will current share with about 2-4A load balance.

4.1 Active current sharing (A.C.S)

Current sharing done in a closed loop. All paralleled outputs are compared and feedback is used to balance their load current. The result is a more stable, less sensitive output voltage without voltage drop. Typical Load Balance of about 2-4A for all Load range is expected.
 ACS is supported by the 12V output. .Optional for 3.3Vaux^{1 2}

4.2 3.3Vaux Passive Current Sharing (P.C.S).

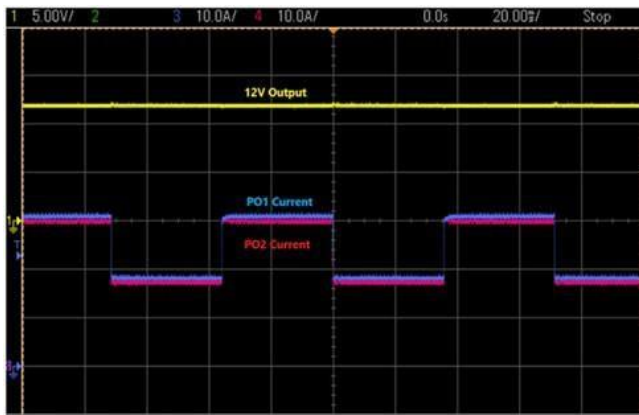
Current sharing is done in open loop, output voltage drops as a function of output load.
 .Load Balance of about 5-10% is expected
 4.3 Vaux ACS is optional^{1 2}

3.3 Current share connection between two Units.

For a required output to current share please connect the following Pins between the two units

- *PO#_Sense & PO#_Sense_RTN* (for best performance, Pins from paralleled units should be connected to a single point and as close as possible to the load point)
- *VSI_SHARE (A7)*
- *VSI_ACS (C7)*
- *3.3Vaux_SHARE (B7)*
- *3.3Vaux_ACS (D1)* Optional^{1 2}

Typical ACS Dynamic Load of Two 12V Paralleled Outputs (PO1 & PO2 refer to two different units)



Notes 1. When Not used, 3.3Vaux A.C.S can be left open.

When ordering 3.3Vaux P.C.S or 3.3Vaux Non-Current Share unit, this pin is Internally disconnected

2. 3.3Vaux ACS (Pin D1) is not required by SOSA and is optional. (Pin was previously on Pin B4)

5. NED

5.1 NED circuit operation

NED Output is Normally Low, goes High After NED detection

NED circuit operation needs to be verified by User

5.2 Power Supply compliance

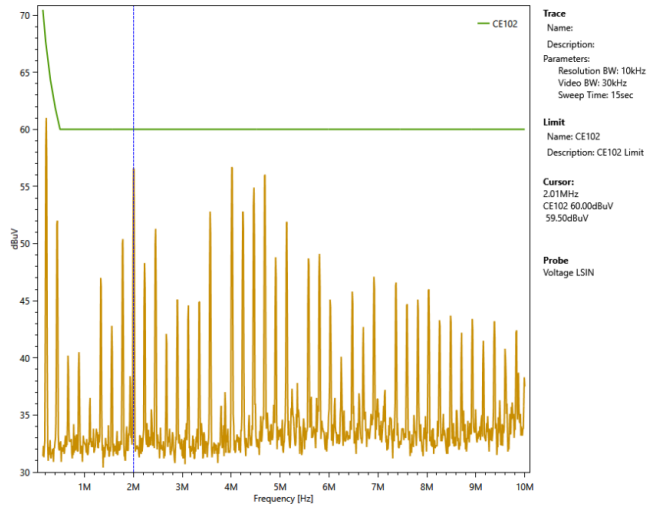
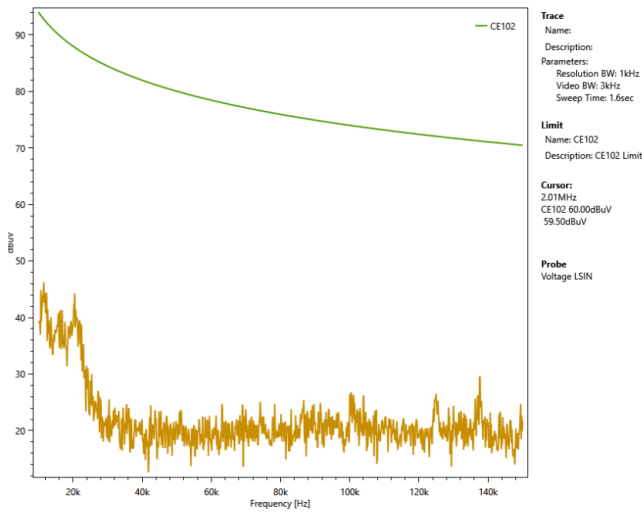
Power supply performance during and after NED event needs to be verified by User.

For additional information, please contact factory.

6. Efficiency



7. EMI CE102 Tests



8. Communication Protocol

Unit communication protocol can be configured as **Vita 46.11 Tier 2 IPMC** or **Custom IPMI** compatible protocol. For more details on protocols refer to para. 6.1 and 6.2

8.1 Custom IPMI Protocol

Electrical Parameters

:Vcc 3.3VDC
 Pull-up: 20kOhm
 Input capacitance: 100pf

Slave Device Addressing

- address spaces 256
- Baud rate: 200kHz maximum
- Bit Protocol 7
- Support Slot Addressing per VITA 62

Slot Number	MSB							R/W
	A6	A5	A4	A3	*A2/GA2	*A1/GA1	*A0/GA0	
Slot0	0	1	0	0	0	0	0	
Slot1	0	1	0	0	0	0	1	
Slot2	0	1	0	0	0	1	0	
Slot3	0	1	0	0	0	1	1	

* Slot location is determined by GAx per VITA 62.

Communications Supported

Read Command – 21Hex, deliver 64Bytes of Data. (More commands are available by request) The communication starts when the master sends a start followed by the unit slave address, command, checksum and a stop. A second start followed by the slave address and a read will be followed by a 64 Bytes response.

S	Slave Address	R/W	A	Command	A	Check sum	A	P
	A6:A0	0	0	Hex 21	0	DF Hex	0	

W															
S	Slave Address	/R	A	DATA	A	DATA	A	DATA	A	...	DATA	A	Check sum	N/A	P
	A6:A0	1	0	D7:D0	0	D7:D0	0	D7:D0	0	...	D7:D0	0	D7:D0	1	

Command – 21Hex read all 64 Bytes

S -Start

P- Stop

Master Transmit	Unit Transmit
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Memory Space

Response # Byte	Data Type	Meaning	Interpretation	Reading Range
0	U Integer, MSB First	Echo of Command		Hex 21
1		N/A		Hex 00
2-3	S Integer, MSB First	Temperature 55C to 120C-	T(C°)=+/- 7bit Dec	55°C to 125°C-
4-5	U Integer, MSB First	12V VS1 Voltage	V(out) = Data · m ₂	20.48V
6-7	U Integer, MSB First	3.3V VS2 Voltage	V(out) = Data · m ₂	20.48V
8-9	U Integer, MSB First	N/A	N/A	N/A
10-11	U Integer, MSB First	N/A	N/A	N/A
12-13	U Integer, MSB First	N/A	N/A	N/A
14-15	U Integer, MSB First	N/A	N/A	N/A
16-17	U Integer, MSB First	12V VS1 Current	V(out) = Data · m ₃	80A
18-19	U Integer, MSB First	3.3V VS2 Current	V(out) = Data · m ₃	20A
20-21	U Integer, MSB First	N/A	N/A	N/A
22-23	U Integer, MSB First	N/A	N/A	N/A
24-35	U Integer, MSB First	N/A	N/A	N/A
26-27	U Integer, MSB First	N/A	N/A	N/A
28-29	U Integer, MSB First	Reserved	00Hex	
30-31	U Integer, MSB First	Reserved	00Hex	
32-51	Character String (ASCII)	Part Number	*M2192-xxx (Note1)	Characters 20
52-53	Decimal, MSB First	Serial Number, 2MSB Dig	X,X Dec (Note2)	Optional
54-55	Decimal, MSB First	Serial Number, 2LSB Dig	X,X Dec (Note2)	Optional
56-57	Decimal, MSB First	Date Code	Week, Year (Note3)	Optional
58-59	Character String (ASCII)	Hardware Rev	B01 & B02 Boards (Note4)	Characters 2
60-61	Decimal, MSB First	Firmware Rev	X,X,X,X Dec (Note5)	digits 4
62	U Integer, MSB First	Reserved		AA Hex
63	U Integer, MSB First	Zero Checksum		Value required to make the sum of bytes 0 to 62 added to a multiple of 256

Note:

M₂ = 20.48/65535

M₃ = 80/65535

M₄ = 20/65535

*Matching unit part number

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Notes 1 to 5

Note 1: Part Number Example: M4465

'Byte No	32	33	34	35	36	37	38	39-51
Character	M	4	4	6	5	(-)	4	0
Hex	4D	34	34	36	35	2D	34	00

Note 2: Serial Number Example: 25

'Byte No	52		53		54		55	
Dec Number	0	0	0	0	0	0	2	5
Binary	"0000"	"0000"	"0000"	"0000"	"0000"	"0000"	"0010"	"0101"

Note 3: Date Code Example: week 35 of 2018

'Byte No	56		57	
Dec Number	3	5	1	8
Binary	"0011"	"0101"	"0001"	"1000"

Note 4: Hardware Rev Example: B01 Rev (-), B01 Rev A

'Byte No	58	59
Character	(-)	A
Hex	2D	41

Note 5: Firmware Rev Example: 2.1.0.0

'Byte No	60		61	
Dec Number	2	1	0	0
Binary	"0010"	"0001"	"0000"	"0000"

8.2 46.11 Tier 2

Please see *46.11 User Manual* for detailed information of operation.

Sensors included are seen in the table below.

Units are designed to be upgradable to 46.11 Tier 3 compliance upon release of that specification

Record ID	Sensor ID	Sensor Type	Name
0000	00	F0h	FRU State Sensor
0001	01	F1h	System IPMB Link Sensor
0002	02	F2h	FRU Health Sensor
0003	03	02h	FRU Voltage Sensor
0004	04	F3h	FRU Temperature Sensor
0005	05	F4h	Payload Test Results Sensor
0006	06	F5h	Payload Test Status Sensor
0100	07	02h	VS1 Voltage
0101	08	02h	VS2 Voltage
0106	0D	03h	VS1 Current
0107	0E	03h	VS2 Current
010C	13	01h	Analog Temperature
9090	N/A	N/A	Device Locator Record
9999	N/A	N/A	Device Management

9. Sync In and Switching Frequency

The unit free running switching frequency while is 220KHz±5%

Unit can be synchronized to External clock signal in frequency range of 200KHz to 300KHz

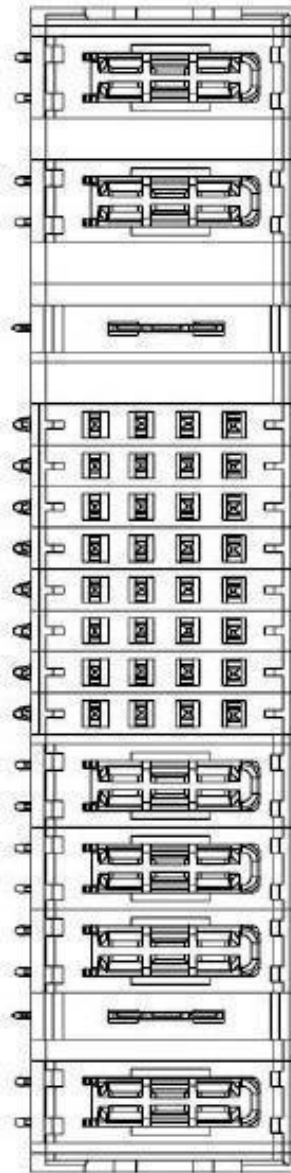
External clock should be 3.3V CMOS standard logic level with duty cycle between 20% to 80%.

The Internal clock will sync after 32, within tolerance, external clock cycles.

Unit will revert to its internal clock upon any out of tolerance external clock and will require another 32 clocks to re synchronized.

Note: Sync_in function is optional, please contact factory if required.

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PART NUMBER	ROWS	POWER								SIGNAL								POWER						
		P1	P2	LP1	1	2	3	4	5	6	7	8	P3	P4	P5	LP2	P6							
6450849-7	D				Z5	Z5	Z5	Z5	Z5	Z5	Z5	Z5	Z5	Z5	Z5	Z5								
	C				Y5	Y5	Y5	Y5	Y5	Y5	Y5	Y5	Y5	Y5	Y5	Y5								
	B	TT	TT	LT	R5	R5	R5	R5	R5	R5	R5	R5	R5	R5	R5									
	A				Q5	Q5	Q5	Q5	Q5	Q5	Q5	Q5	Q5	Q5	Q5	Q1								

2ACP+ILP+32S+3HDP+ILP+1HDP

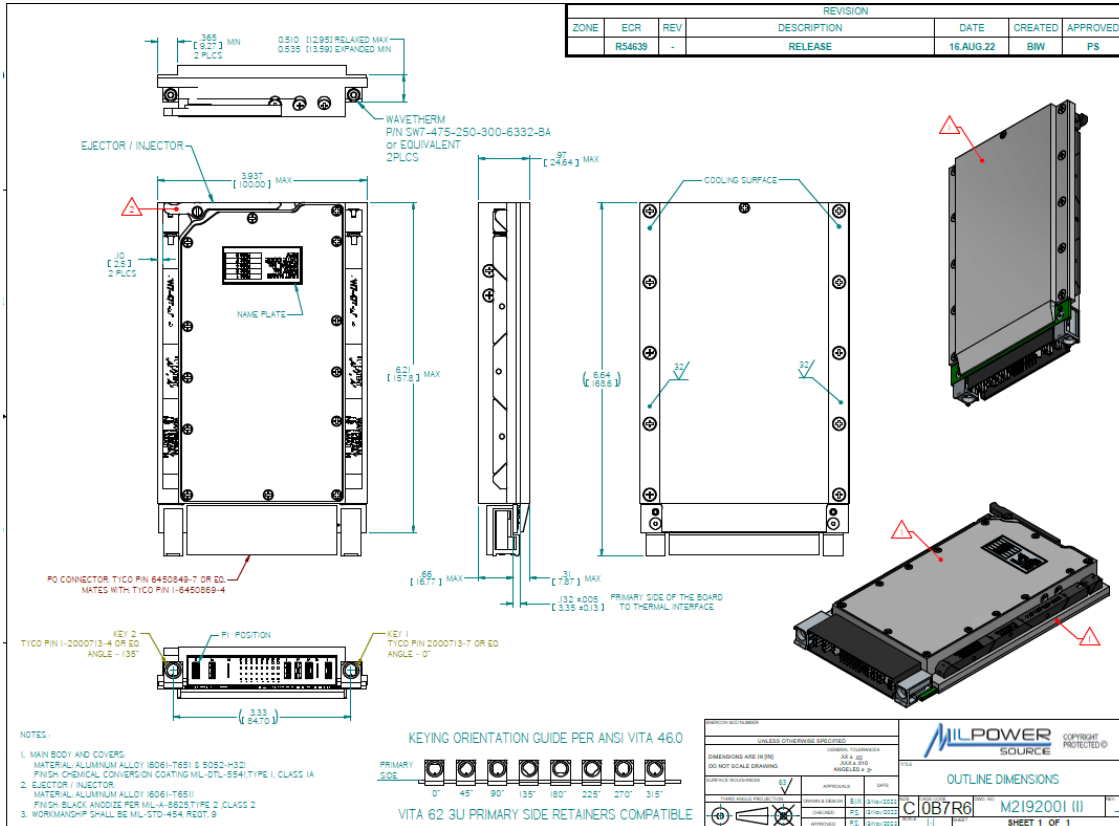
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Pin Assignments

Pin Number	Pin Name
P1	DC_IN-
P2	DC_IN+
LP1	CHASSIS
P3	VS1
P4	POWER_RETURN
P5	POWER_RETURN
LP2	3.3Vaux
P6	VS1
A8	VS1_SENSE
B8	3.3Vaux_SENSE
C8	N.C (VS1_SENSE)
D8	SENSE_RETURN
A7	VS1_SHARE
B7	3.3Vaux_SHARE
C7	VS1_ACS
D7	Sig_RTN
A6	SCL_B
B6	SDA_B
C6	.N.C
D6	*SYSRESET
A5	*GA0
B5	*GA1
C5	SCL_A
D5	SDA_A
A4	.N.C
B4	.N.C
C4	N.C
D4	N.C
A3	.Sync_In / N.C
B3	.N.C
C3	NED
D3	NED RETURN)
A2	.N.C
B2	*FAIL
C2	*INHIBIT
D2	*ENABLE
A1	.N.C
B1	N.C
C1	*GA2
D1	.3.3Vaux_ACS / N.C

M2192 Series– DC/DC Power Supply

Outline Drawing



Notes

1. Dimensions are in Inches[mm]
2. :Tolerance is
XX.±IN 0.02
XXX.±IN 0.008
3. .Weight: Approx. 830g (29.28) oz
4. 3D model available

* Specifications are subject to change without prior notice by the manufacturer.

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