# M4096 SERIES

## Power Supply Data Sheet

### 3U VPX 270V 830W SOSA Aligned

### VITA 47 CCW7 NT4 V3 OS2 C4 AV2 SF1/2/3 CS5

***Key improvements over the M4094:***
*Improved Efficiency*
*Increased Power*
*Improved Thermal Performance*
*Output Sequencing*
*SOSA Drivers Compatibility*
*Upgraded 46.11 Protocol (Compatible IPMITOOL, ELMA ChM)*
*In-Field Secured programming*
*Two Level ESD protection*

## Product Highlights

- **VITA 62.2**
- **SOSA™ ALINGED**
- **Ruggedized**
- **830W Output Power**
- **Operational -55°C to 85°C at unit edge**
- **EMI: Mil-STD-461G**
- **Environmental: MIL-STD-810H**
- **Supports Mil-STD-704 Abnormal Transient**
- **Cyber Secure**
- **DO254 upgradable**
- **Milpower Technical Support**

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## 1. Scope

The M4096 Power supply is a member of Milpower SOSA Aligned VPX product line and is intended to serve at High Input DC line to support a total of 800W steady state, under all operational Line and temperature conditions.

## 2. Module High Level Specification Details

Milpower Part Number **M4096**

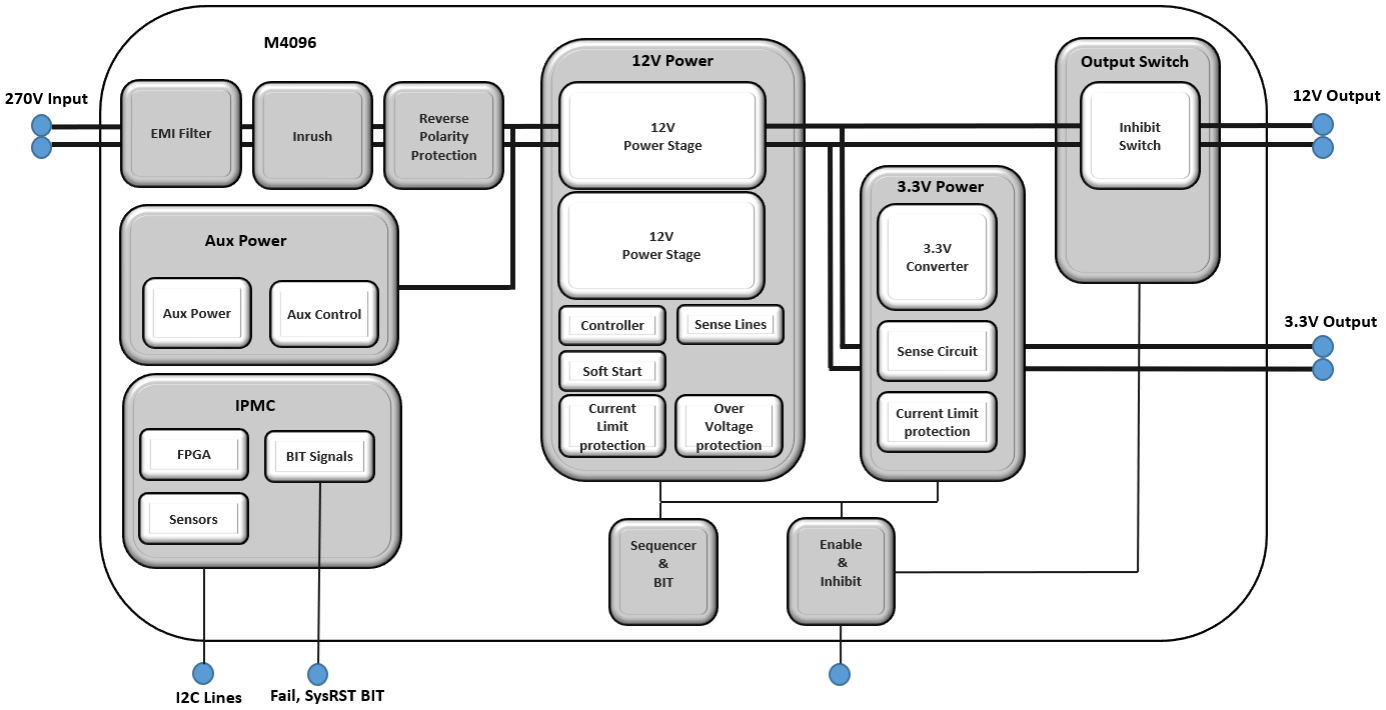
| Parameter | Functionality |
|---|---|
| Form factor | 3U VPX, VITA 65 compliant 1: pitch |
| Cooling | Conduction cooled |
| Power input | 270V Line, Mil-STD-704 |
| Power output | 12V/64A, 3.3V/20A, 830W |
| System Management | Tier-II IPMI/46.11 via P0 IPMI-A and IPMI-B ($I^2C$ level) ports<br>FPGA based management (JTAG USB is on board. 3.3V to 5V Level only, 5V max) |
| Temperature | -55C – 85C, conduction cooled |
| Weight | Approx 800g |

### 2.1 Special Features

- VITA 62.2
- Aligned with the SOSA™ Technical Standard
- VITA 47 CCW7 NT4 V3 OS2 C4 AV2 SF1/2/3 CS5
- ESD Protection
- Wide Input Range
- VITA 62.2 connectors for increased Breakdown Voltage
- Up to 830W output power without derating
- Active Current Share
- Remote Sense
- Outputs Short Circuit Protection
- Outputs Over Voltage Protection
- Over Temperature Shutdown with Auto Recovery
- Design for Mil-STD-461-G
- System Management: protocol per VITA 46.11 (IPMI Tool, ELMA ChM)

## 3. M4096 Power Supply Operation

### 3.1 Unit Block Diagram




**M4096 detailed block diagram**

## 3.2 Electrical Specification

**DC Input Mil-STD-704:**
- Mil-STD-704
  Detailed information on Para 3.5.1.1
- Mil-STD-1275 100V Surges.
- Extended Compliance Optional

**DC Outputs:**
- VS1: 12V / 64A
- 3.3Vaux: 3.3V / 20A

**Isolation:**
- 500V Input to chassis.
- 500V Input to Output
- 100V Output to chassis

**Line Load Regulation**
- 12V Output 11.85V to 12.15V
- 3.3V Output 3.28V to 3.42V,
  3.25V to 3.45V parallel, PCS.

**Efficiency**
Up to 92%, Typical.

**EMC**
Mil-STD-461G:
CE101, CE102, CS101, CS114, CS115, CS116

**Ripple and Noise**
Typical less than 50mV (max 1%).
Measured on load after 1 ft harness across 0.1µF capacitor, with 10 µF on Load.

**System Management Options:**
- Simplified IPMI
- IPMC Tier 2
  (Tier 3 Upgradable)

**Typical Quiescent Current**
- Inhibited Output 20mA (3.3Vaux only).
- Disabled Outputs 17mA (Outputs Off).

**Load Transients**
Outputs dynamic response less than 5% for Load steps 60% - 90%.
Outputs return to regulation <1mSec.

### 3.2.1 Protections

**Input Current Inrush:**
- EMI Filter capacitance ≈ 1µF.
  1A inrush for DO160F 300µSec Input rise time.
- Bus Charge Inrush < 3A@1mSec
- Output Turn-on, Input current < 0.1A

**Outputs Over Voltage**
- 12V Active OVP
- 3.3Vaux Active OVP

**Overload Protection:**
Hiccup Over-load / Short Circuit Protection. Typically, 110%-130% Load.

**Input Under /Over Voltage Protection**
- Under Voltage Turn-off 170V-180V[1, 2]
- Over Voltage Turn-off 370V-380V[1, 2]
- Supports Transients per 3.5.1.1

*Note:*
*1. Extended Compliance Optional*
*2. More details on Para 3.5.1.1*

**Over Temperature Protection**
Thermal shutdown at Internal temperature of 95±5°C, Auto Recovery 90±5°C

## 3.3 Environmental Specification.

### VITA 47 CCW7 NT4 V3 OS2 C4 AV2 SF1/2/3 CS5

**Temperature:**
- Operational -55°C to 85°C (Unit Edge)
- Exceed Vita 47 CC4.
- Storage -55°C to 125°C
- Designed to meet 600 Thermal Cycles

*Note: Plug-in unit surface temperature is measured on the unit edge*

**Altitude:**

Method 500.5 procedure I & II
- Storage / Air Transport: 40kft
- Operation / Air carriage: 70kft

**Rapid Decompression**

Designed to meet per Vita 47.1

**Corrosion Resistance**
- Mil-STD-810G, Method 509.5.
- VITA47 Class SL1/2/3 [1,2]

*Note:*
1. *When not installed in chassis, residues might be accumulated on pins.*
2. *When not installed in chassis, anodized frame is recommended*

**Fungus**

Does not support Fungus growth per Mil-HDBK-454, Guideline 4.

**Humidity**
- Mil-STD-810G, Method 507, up to 95% RH.
- 100% condensation, consult factory.

**Vibration & Shock**
- Vita 47 Vibration Class V3.
- Vita 47 Operational Shock Class OS2
- Vita 47 Bench Handling Shock

**ESD**
- Designed to meet per VITA 47.1

**Coating**
- Humiseal 1A33.
- Parylene optional.

**Reliability**

375,135 Hours,
calculated IAW MIL-HDBK-217F Notice 2
at +65 ℃, GF

**ESS**

Environmental Stress Screening available, please contact factory for available options.

## 3.4 Unit Interfaces

### 3.4.1 Connectors

| | | |
|---|---|---|
| **Front Panel Connector**<br><br>**Mating Connector** | TE 2313442-1 or equivalent<br><br>TE 2313441-1 or equivalent | Main Connector<br><br>Backplane Connector |
| **Wedge Locks** | WAVETHERM SW7-475-250-300-6332-BA | |
| **Key 1**<br><br>**Key 2** | 1-1469492-8 or equivalent<br><br>1-2000713-4 or equivalent | 315°<br><br>135° |
| **Back Panel USB-C Port** | USB Type-C | FPGA Programing Port (5V Abs) |

### 3.4.2 Functions and Signals

| Signal Name | Type | Description |
|---|---|---|
| FAIL* | Output Open Drain | Indicates to other modules in the system that a failure has occurred in one of the outputs. [1, 2, 3] |
| SYSRESET* | Output Open Drain | Indicates to other modules in the system that an output voltage is not in its nominal range. [1, 2, 3] |
| INHIBIT* | Input | Controls 12V Output. [1] |
| ENABLE* | Input | Controls 12V, 3.3V Outputs. [1] |
| GA0*, GA1*, GA2* | Input | System addressing per VITA46. [1] |
| SCL_A, SDA_A | buffer | Primary $I^2C$ lines. [1] |
| SCL_B, SDA_B | buffer | Secondary $I^2C$ lines. [1] |
| SYNC IN | Input | External Clock for PWM Synchronization. [1] |
| PO_SENSE | Output | Output Sense line for voltage compensation. |
| SENSE RETURN | Output | Output Sense return for voltage compensation. Common line for all outputs. |
| SHARE | Bi-Directional | Current share pins |
| 3.3V AUX ACS | Bi-Directional | Additional Current share pin to support 3.3VAux Active Current Share. |
| SIGNAL RETURN | Passive | Return path for all signals, refers to Output Power ground. |

**General Note:**

Signal Levels per VITA 62

*Notes:*

1 Refers to SIGNAL RETURN

2 Maximum current of 80mA (minimum total pull-up resistance > 42ohm)

3 See para 3.5.3.1 for additional information

## 3.5 Power Detailed Description

### 3.5.1 Input Voltage

#### 3.5.1.1 Operational Input Range

The M4096 input Voltage range for Mil-STD-704 is given at table 3.5.1-1.
Unit will be fully operational under all steady state condition and will be protected or ride-through various transients.
In case ride-through transient duration exceeds a 4 Sec duration, the unit will automatically shut-down with auto recovery before the input voltage returns to steady state. Protection shut-down duration as a result of input transients is approximately 1 Sec OFF time.
After shut-down, the unit will recover before input voltage is back to steady state.
When first applying Input voltage, the unit will turn-on before reaching steady state voltage.

| Condition | Mil-STD-704 | 704A | 704B | 704C | 704D | 704E | 704F |
|---|---|---|---|---|---|---|---|
| **Normal Steady State Voltage** | **HDC102** | N/A | Operational | Operational | Operational | Operational | Operational |
| **Voltage Distortion Spectrum** | **HDC103** | N/A | | | | Pass | Pass |
| **Total Ripple** | **HDC104** | N/A | | | | | |
| **Normal Voltage Transients** | **HDC105** | N/A | Protected | Protected | Protected | Ride-through | Ride-through |
| **Power Interrupt** | **HDC201** | N/A | Protected / Ride-through with M4262 Hold-up unit | | | | |
| **Abnormal Steady State Voltage** | **HDC301** | N/A | Operational | | | | |
| **Abnormal Voltage Transients** | **HDC302** | N/A | Protected | | | | |
| **Emergency Steady State Voltage** | **HDC401** | N/A | Protected | Protected | Protected | Ride-through | Ride-through |
| **Starting Voltage Transients** | **HDC501** | N/A | Protected | | | | |
| **Power Failure** | **HDC601** | N/A | Protected | | | | |
| **Phase Reversal** | **HDC602** | N/A | Protected | Protected | Protected | Protected | Protected |

**Table 3.5.1.1-1 Operational Range**

*Notes:*

1. For extended Input Range, please contact factory.
2. For additional information regarding Mil-STD-704A please contact factory.

### 3.5.1.2 Transient Response

Power supply is designed to have a good transient response for input voltage transient
An Example of 704F QQ and RR transient under full load is given below

| Combined Transient | | | | | |
|---|---|---|---|---|---|
| QQ | 280 Vdc<br>then | < 1 msec<br>< 1 msec | 200 Vdc<br>330 Vdc | 10 msec<br>20 msec | < 1 msec<br>20 msec |
| RR | 250 Vdc<br>then | < 1 msec<br>< 1 msec | 200 Vdc<br>330 Vdc | 10 msec<br>20 msec | < 1 msec<br>33 msec |

Table

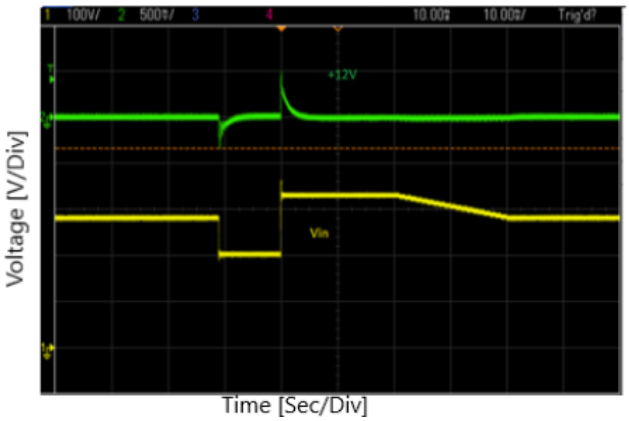



**Figure3.5.1-1. 12V response for QQ transient**

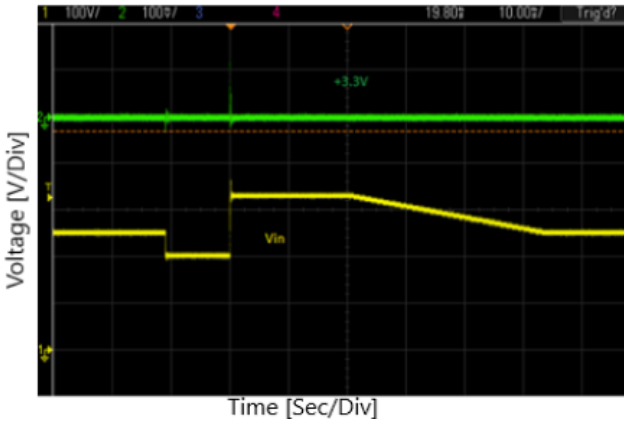



**Figure3.5.1-2. 12V response for RR transient**

### 3.5.1.3 Voltage Distortion

Unit verified per Mil-HDBK-704-8 HDC103

| System Test | | | | | | | |
|---|---|---|---|---|---|---|---|
| **CONDITION** | | | **LIMITS** | | | | **RESULTS** |
| **270V With Load** | | | +3.3VS2/20A | | +12VS1, VS3/64A | | |
| **Test** | **Frequency** | **Voltage rms** | Vout 3.28V ÷ 3.42V | Ripple ≤ 50mV | Vout 11.85V ÷ 12.15V | Ripple ≤ 120mV | |
| **A** | **10Hz** | **0.316** | 3.33 V | 5 mV | 12.00 V | 10 mV | Pass |
| **B** | **25Hz** | **0.500** | 3.33 V | 5 mV | 12.00 V | 10 mV | Pass |
| **C** | **50Hz** | **0.562** | 3.33 V | 5 mV | 12.00 V | 10 mV | Pass |
| **D** | **60Hz** | **0.775** | 3.33 V | 5 mV | 12.00 V | 15 mV | Pass |
| **E** | **250Hz** | **1.581** | 3.33 V | 5 mV | 12.00 V | 25 mV | Pass |
| **F** | **1KHz** | **3.162** | 3.33 V | 5 mV | 12.00 V | 35 mV | Pass |
| **J** | **1.7KHz** | **3.162** | 3.33 V | 5 mV | 12.00 V | 35 mV | Pass |
| **H** | **2KHz** | **3.162** | 3.33 V | 5 mV | 12.00 V | 35 mV | Pass |
| **I** | **5KHz** | **3.162** | 3.33 V | 5 mV | 12.00 V | 60 mV | Pass |
| **J** | **6.5KHz** | **2.433** | 3.33 V | 5 mV | 12.00 V | 90 mV | Pass |
| **K** | **10KHz** | **1.581** | 3.33 V | 5 mV | 12.00 V | 20 mV | Pass |

### 3.5.1.4 Input Redundancy

M4096 can support parallel operation while fed from two independent power sources.
Please note: this configuration does not guarantee output redundancy during short on outputs.

### 3.5.1.5 Input Voltage Rise Time

There is no limitation on Input voltage rise time, contactor connection is supported.

### 3.5.1.6 Inrush Currents

Turn-on inrush current can be divided into 3 categories:

**EMI Filter charge Inrush,** input current, is a function of input voltage rise time, charging the EMI filter 1µF capacitance. Per DO160F, rise time of 300µSec will result in an inrush current of less than 1A.

**Bus charge Inrush**, charging Bus capacitance, controlled by the Unit Inrush circuit with Typical current lower than 3A with a duration of about 3mSec. See Figure 3.5.1.6-1.

**Turn-on Inrush,** Input current while outputs turn on, typical lower than 0.1A. See Figure 3.5.1.6-2.


**Figure 3.5.1.6-2 Outputs Turn-on Inrush.**
**<0.1A Input Inrush current with 12V Loaded.**

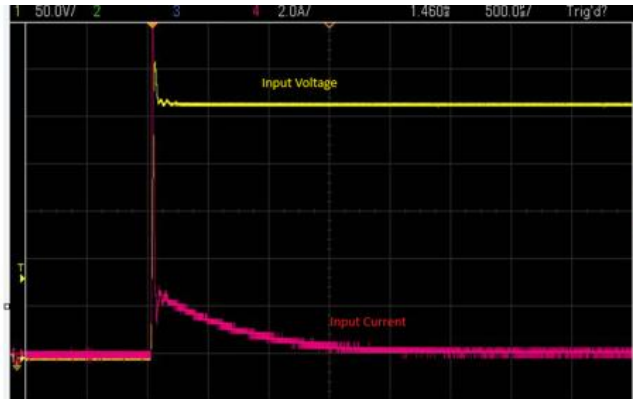



**Figure 3.5.1.6-1 Bus Charge Inrush**

### 3.5.2 Output

#### 3.5.2.1 Output Controls: Enable & Inhibit Signals

Outputs are controlled by Enable and Inhibit Signals per VITA 62 definition. See Table 3.5.2.1-1

| INHIBIT* | Low | Low | High | High |
|---|---|---|---|---|
| ENABLE* | Low | High | Low | High |
| 12V Output | OFF | OFF | ON | OFF |
| 3.3V Aux Output | ON | OFF | ON | OFF |

**Table 3.5.1.1-1 Outputs Truth table per Signal Status**

#### 3.5.2.2 Output Power

Standard configuration will support 12V/64A and 3.3VAux/20A with up to 2mF capacitance on each output.
No Power-derating is required for current share application.
*Note:* for extended output capacitance, please contact factory.

#### 3.5.2.3 Voltage regulation and Ripple

Volage regulation and ripple are measured as sense point location and limits are under all operational range (Line, Load, Temperature). Limit is also given for ACS (12V, 3.3Vaux optional) and 3.3VAux PCS.

Voltage is measured at connector output, Sense line shorted to output.

| Statues | 12V Output Limits | 3.3VAux Output Limits |
|---|---|---|
| Single Unit | 11.85V – 12.15V | 3.28V – 3.42V |
| Current Share (3.3VAux ACS) | 11.85V – 12.15V | 3.28V – 3.42V |
| Current Share (3.3VAux PCS) | 11.85V – 12.15V | 3.25V – 3.45V |

**Table 3.5.1.2-1 Outputs Voltage Regulation under all Line, Load and Temperature**

*Note:* limits above are under all Line, Load and Temperature steady state condition

| Statues | 12V Output Limits | 3.3VAux Output Limits |
|---|---|---|
| Single Unit | 120mV | 50mV |
| Current Share (3.3VAux ACS) | 120mV | 50mV |
| Current Share (3.3VAux PCS) | 120mV | 50mV |

**Table 3.5.1.2-2 Outputs Voltage Ripple under all Line, Load and Temperature**

*Notes:*

1. Limits for 250V-280V Input, under all Loads and Temperature conditions
2. Ripple is measured on load after 1 ft harness across 0.1µF capacitor, with 10 µF on load (20MHz BW).

### 3.5.2.4 Turn-on & Sequencing

Unit can support sequencing between 12V and 3.3Vaux, standard configuration would have the 3.3Vaux Turn-on about 50mSec prior to 12V Output.

Typical Turn-on under various conditions is given in *Figures 3.5.2.4-1 through 4*

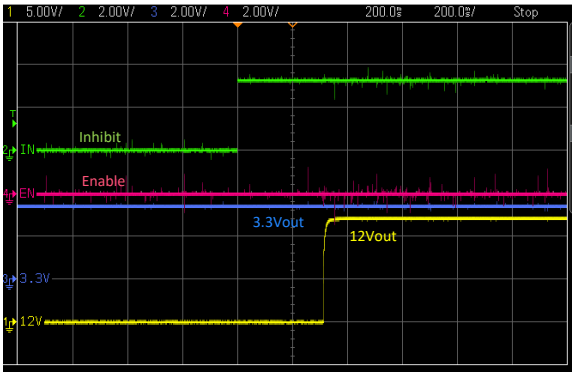



**Figure 3.5.2.4-1. Inhibit Turn-on**

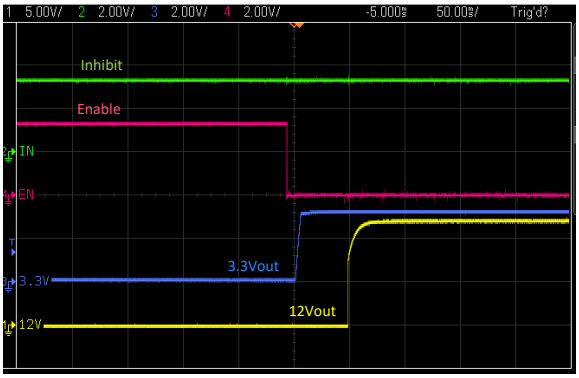



**Figure 3.5.2.4-2. Enable Turn-on**

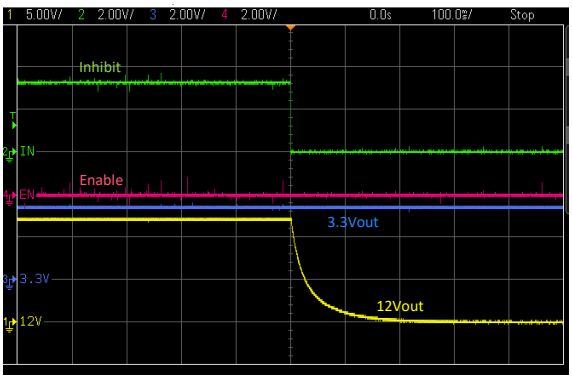



**Figure 3.5.2.4-3. 12V Inhibit Turn-off**

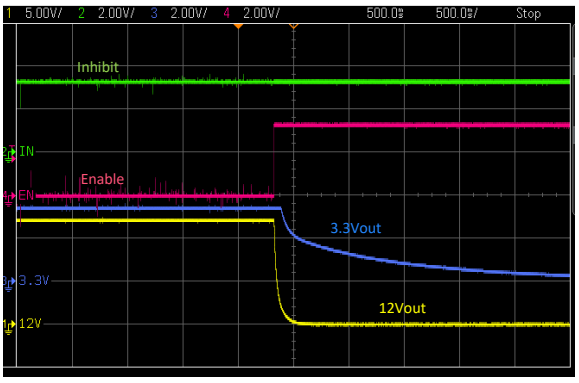



**Figure3.5.2.4-4. Enable Turn-off**

### 3.5.2.5 Sense Connection

Sense lines are provided for 12V and 3.3Vaux outputs for line voltage drop. Each output has its own sense line with a single SENSE RETURN signal. Recommended connection shown on *Figure 3.5.2.5-1* A8, C8 are redundant 12V Sense lines, B8 is the 3.3Vaux Sense line and D8 is the common-sense return.
Unit sense circuit can compensate up to 0.4V at full load.

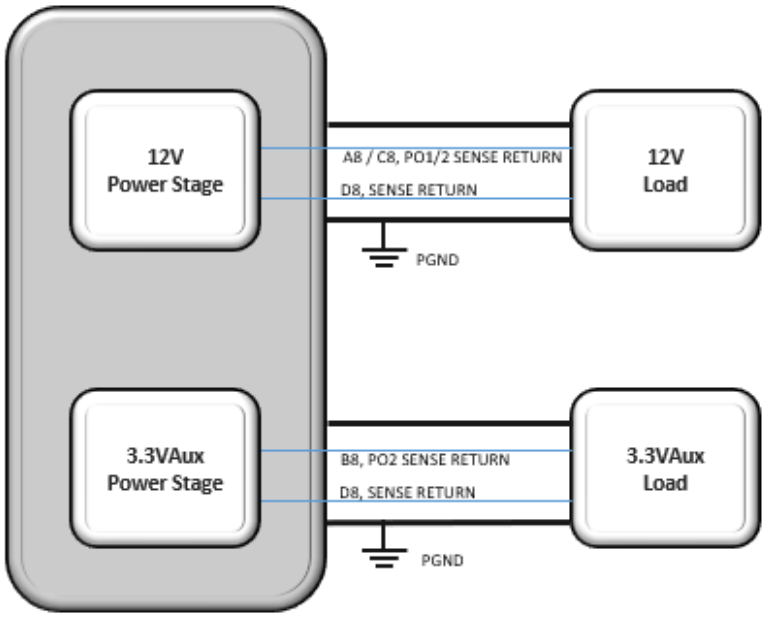



**Figure 3.5.2.5-1. Output's sense connection**

### 3.5.2.6 Dynamic Response

Typical performance of a 60% to 90% load dynamic response

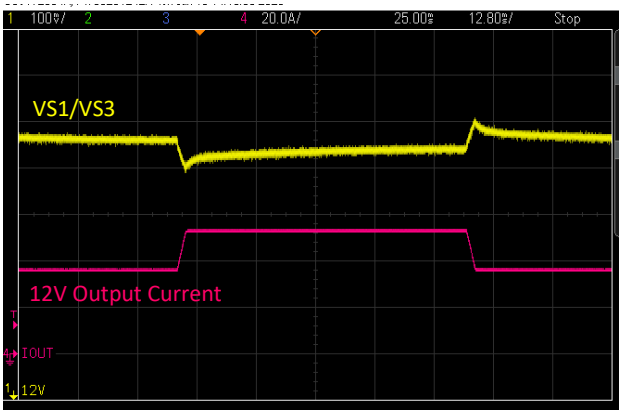



**Figure 3.5.2.6-1. 12V Dynamic Response**

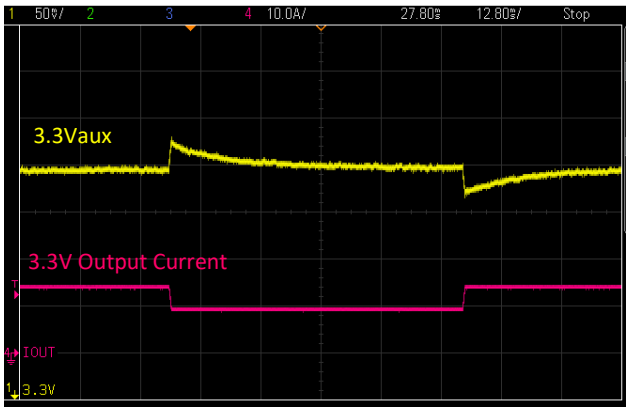



**Figure 3.5.2.6-2. 3.3V Dynamic Response**

### 3.5.2.7 Current Share

Current share allows the user to connect two or more M4096 units in parallel to increase the output power of each rail. No derating is required for current share configuration.
Current share typically provides up to 1-3A balance between unit.
An example of 2 M4096 units, each providing about 60A is given in Figure *3.5.2.7-1.*

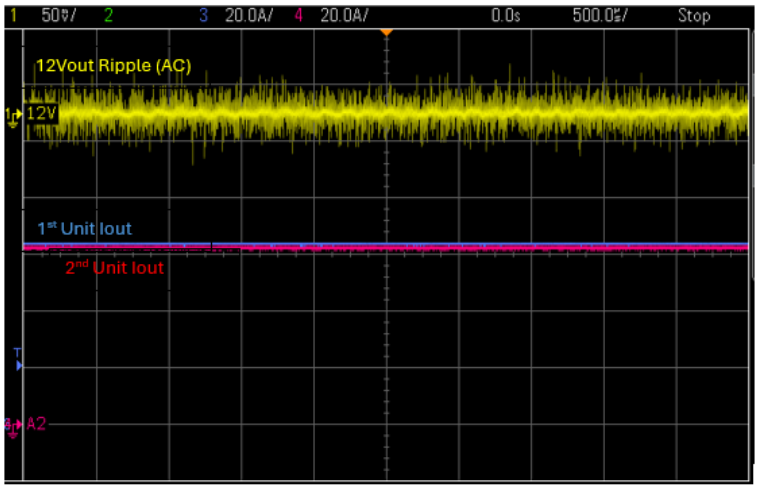



**Figure 3.5.2.7-1 (2 units) Current Share with Output Ripple**

The 12V output is using Active Current Share topology. By comparing the actual current between paralleled units, the unit can provide accurate share balance between outputs with very low susceptibility to power traces and sense connection and no need for voltage drop.
The 3.3Vaux output supports both Passive Current share with voltage drop or ACS with an additional U.D pin.
During a fault condition for both ACS or PCS, both relative outputs will hiccup synchronously to support synchronous turn on into load.
Recommended current share connection is given on *Figure 3.5.2.7-3*

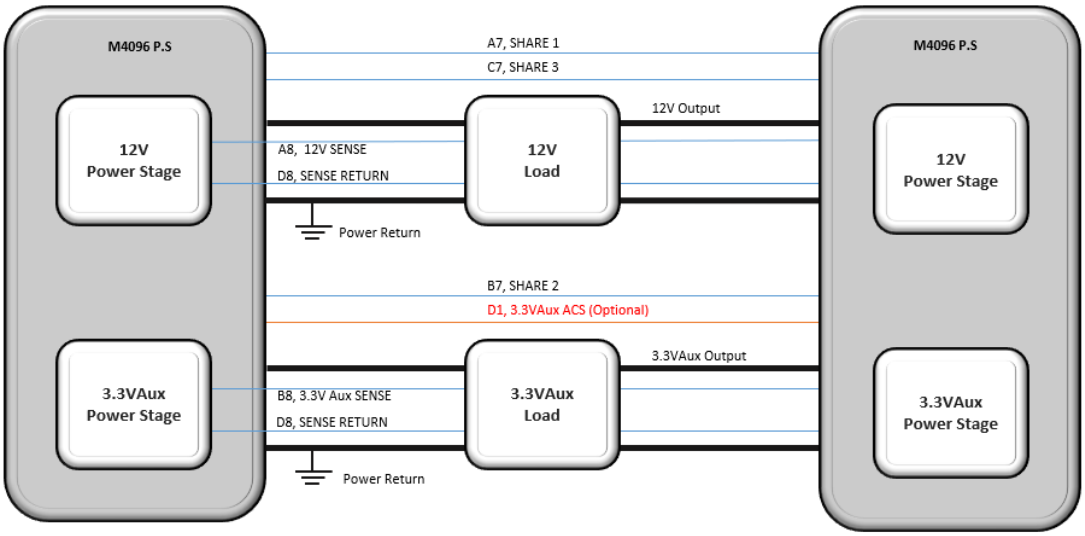



**Figure 3.5.2.7-3 current share connection.**

Note: For best current share balance, make sure both outputs SENSE lines are connected to a single load point to insure Vout of each outputs is as close as possible to the other.

Please note:

- Current share is an optional configuration.

  For current share configuration, the 12V is ACS, 3.3V can be either PCS or ACS.

  3.3VACS requires the use of D1(UD4) pin
- Typically, current share starts at load above 10% of max load
- No derating required when connecting units in parallel.
- Current share is not a guarantee for redundancy, some failures (E.g. short on output) will result in a failure of both units.
- During Overload condition, both relative outputs will be synchronized with their hiccup to allow Turn-on into full load once the fault condition is removed.
- Multiple current share units are optional

#### 3.5.2.8 Short Protection

Both 12V and 3.3VAux outputs have an indefinite hiccup for over-Load / short circuit protection. The over-load hiccup threshold is 110%-120% of nominal current. Output will automatically recover after removal of fault condition.
A short on 3.3VAux rail will not affect the 12V Output, a short on the 12V rail will cause the 3.3VAux to hiccup as well.

While output is at hiccup mode, current during on-time may exceed 140% of max current.

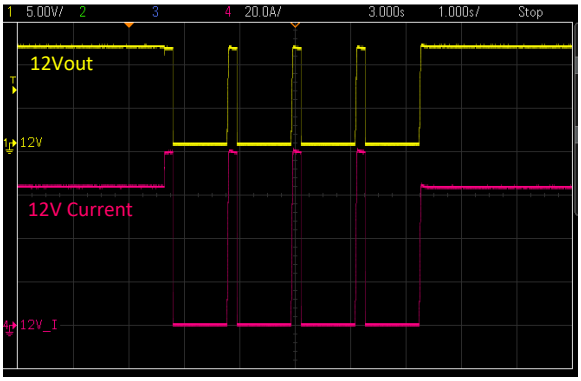



**Figure 3.5.2.8-1 12V Output hiccup and recovery after short**

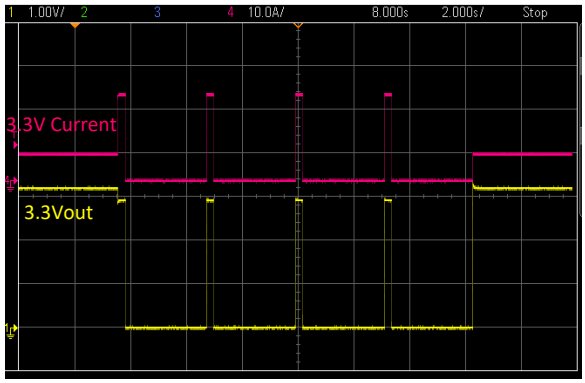



**Figure 3.5.2.8-2 3.3V Output hiccup and recovery after short**

#### 3.5.2.9 Over Voltage Protection

Both 12V and 3.3VAux outputs have active Over Voltage Protection. An O.V. condition, caused by internal failure will cause the relevant output to Shut down, with Auto recovery.

| Output | **Shutdown** | **Recovery** |
|---|---|---|
| **12V** | 13.2—13.6V | 12.4—12.6V |
| **3.3Vaux** | 3.8—4.0V | 3.8—4.0V |

Note: 12V OVP will shutdown 3.3VAux as well.

### 3.5.3 Signals

#### 3.5.3.1 Fail BIT & SYSTEM RESET

Unit has two dedicated Fault signals per VITA 62:
**Fail BIT:** Indicates that one of the power supply outputs is out of its normal operating range, with respect to the expected value depending on Inhibit & Enable status.
Signals is Open Drain outputs (Per VITA 65), Normally Open and is driven Low during Fail event.
**SYSTEM RESET:** Indicates to the System that one of the power supply outputs is out of its nominal range.
Signal is Open Drain output (Per VITA 65), Normally Open and is driven Low when output is out of nominal range.
*Note:* for the M4096 this BIT standard configuration is as "Output".

Fail BIT & SYSTEM RESET responses under different conditions are given under Figures 3.5.3.1-1 to 5.
*Note*: Test setup for BITs conditions are using unit's 3.3VAux output as pull-up.

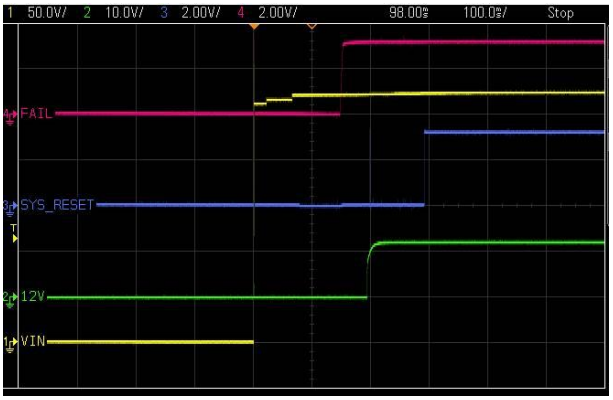



**Figure 3.5.3.1-1 BITs status during Input voltage Turn-on**

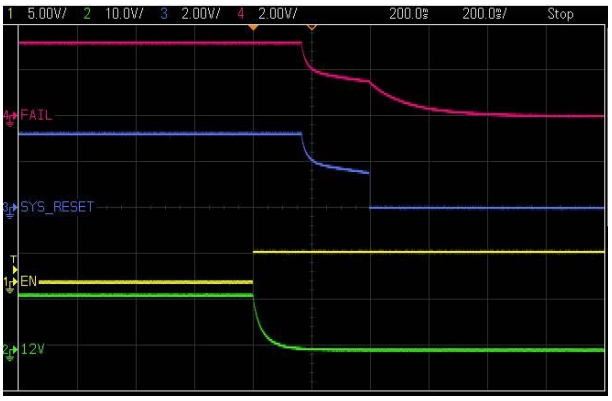



**Figure 3.5.3.2-2 BITs status Enable Turn-off**

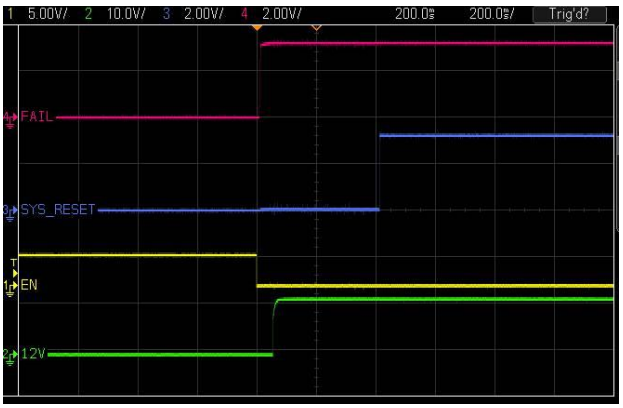



**Figure 3.5.3.2-3 BITs status Enable Turn-on**


**Figure 3.5.3.2-4 BITs status Inhibit Turn-off**


**Figure 3.5.3.2-5 BITs status Inhibit Turn-on**

#### 3.5.3.2 SYNC IN

This pin can be used to synchronize the power supply switching frequency to an external clock. Standard switching frequency with no Sync In signal applied is 120KHz input stage / 220kHz ±5% Output Stage. When configured to use Sync, the unit will synchronize to a signal between 200kHz and 300kHz ±5%. The square wave must be at 3.3V CMOS standard logic levels with a duty cycle between 20% and 80%. The M4096 will sync after 32 cycles within tolerance of an external clock. The unit will revert to its internal clock frequency upon any out-of-specification clock cycles and will need 32 good cycles to resync to the external clock. Contact factory to add Sync_in functionality and to customize its configuration values.

*Notes:*

1. Functional is optional, please contact factory.
2. When not used, keep open.
3. Deviating from original frequency may affect efficiency.

#### 3.5.3.1 SYNC OUT

External Clock for synchronization of two power supplies to the same switching frequency.
If required, please connect SYNC OUT of one unit to SYNC IN of the second unit.

#### 3.5.3.2 NVMRO

NVMRO is used to activate write-protection into the device FPGA. Keep the input pin open or pull high to Enable write protect.
Unit has an internal Pull-up.

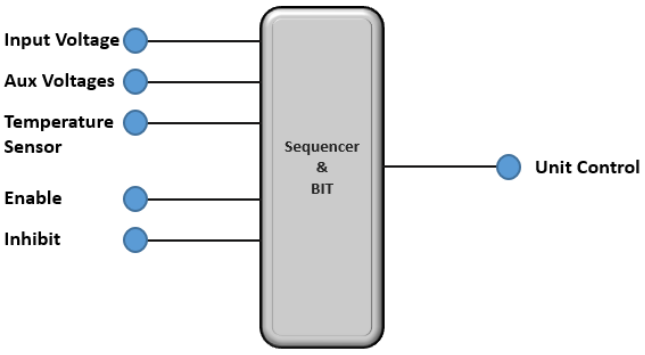
#### 3.5.3.3 Enable & Inhibit

See section 3.5.2.1

### 3.5.4 Built In Tests

For proper operation, the unit has Built In Test circuit, which continuously monitors Unit's internal functions, such as: Input Voltage, Internal Aux voltage, Temperature, Output voltages and control proper Turn-on and Turn-off Sequence.

**Turn on:** verification that all parameters are within normal operating range and all Aux voltages are stable before starting the outputs Turn-on sequence.
**Continuous:** Monitoring all critical parameters and initiates a controlled Turn-off sequence when required.



### 3.5.5 Thermal Management

Operational Temperature range is -55°C to +85°C on the surface of the edge that contacts the rack/enclosure. The contacting surface on the rack needs to be at lower temperature to account for thermal resistance between the unit and the chassis/cold plate. The M4096 wedge thermal interface is 0.1 °C/W per Card Edge. The thermal design of the unit will provide a balanced power dissipation between both sides of the unit.

There are two thermal sensors in the unit:
**$I^2C$ thermal sensor** for 46.11 reporting.
**Analog Thermal Sensor** for protection and shutdown. Shutdown temperature would be between 90°C to 105°C, at unit edge, load dependant.
No power derating is required for all operational temperature range.

### 3.5.6 Efficiency

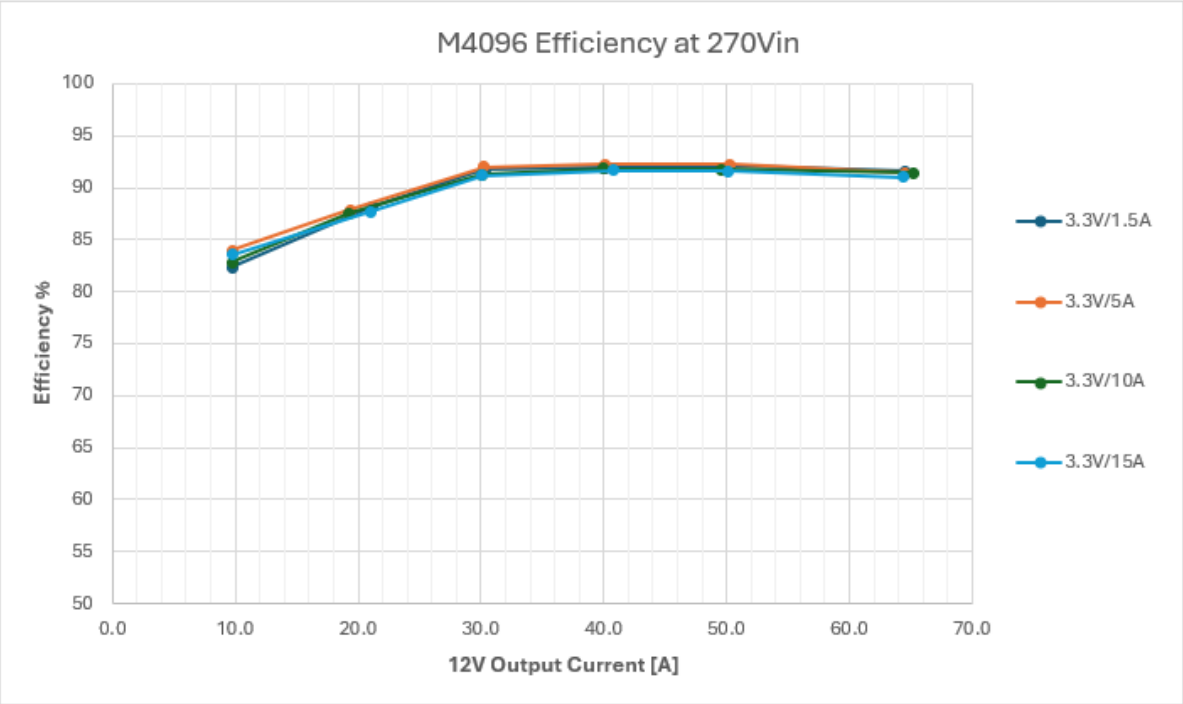



**Figure 3.6-1 Typical efficiency, room temperature**

### 3.5.7 EMI

EMI Test per Mil-STD-461G for CE101, CE102

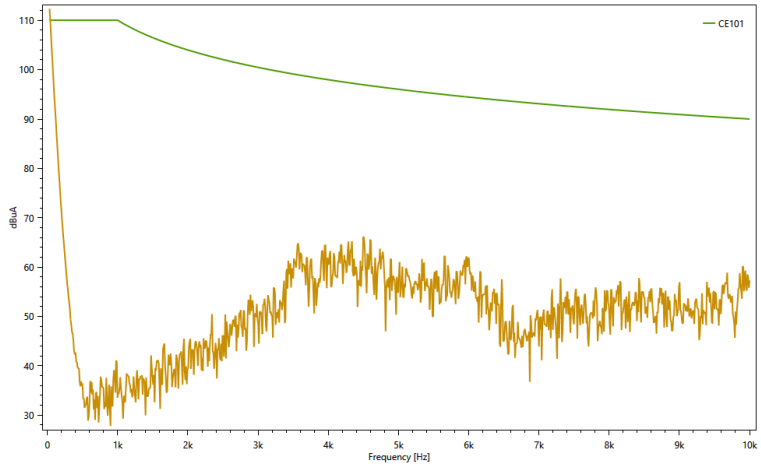



**Figure 3.5.7-1. CE101 Full Load**

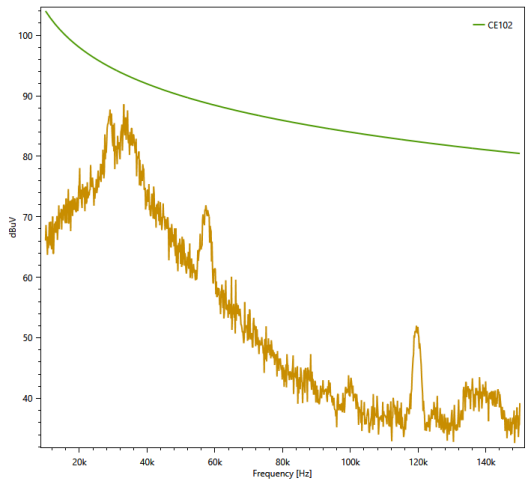



**Figure 3.5.7-2. CE102 10KHz to 150KHz Full**

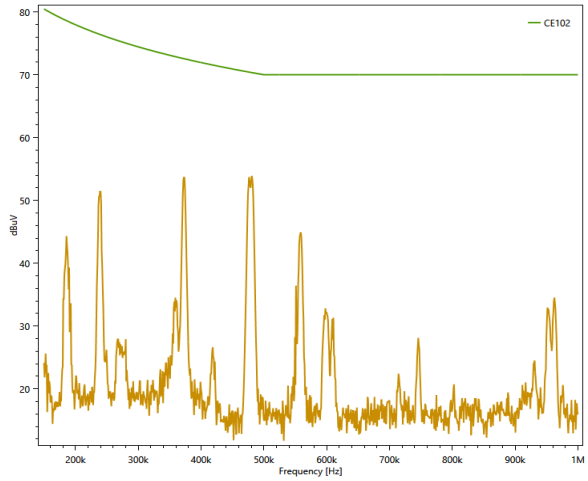



**Figure 3.5.7-3. CE102 150Kz to 1MHz Full**

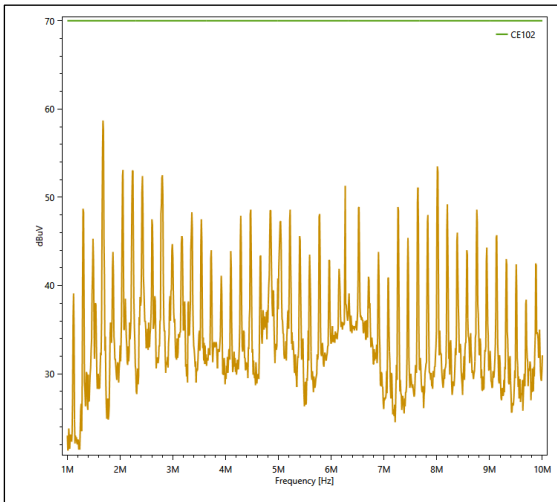



**Figure 3.5.7-4. CE102 1MHz to 50MHz Full**

## 3.6 System Management

### 3.6.1 Electrical Interface

| | |
|---|---|
| **I²C Buffers** | LTC4300 |
| **Pullups** | 20KΩ |
| **Vcc** | 3.3V |
| USB-C Port | Jedec Programing<br>3.3V to 5V Level only, 5V Abs max rating |

### 3.6.2 Communication Protocol

The M4096 can be configured to be one of the two I²C communication protocols: 46.11 Tier 2 IPMC or Advanced I²C.
Slot location, for both options, is defined by VITA62. See table 3.7.2-1.
There following data Sensors are available:
**Output Current sensors**: Max error of +/-5% or up to +/-1A (the bigger of the two)
**Output Voltage sensors**: Max error up to +/-0.2V
**Input Voltage sensors**: Max error up to +/-5V
**Temperature sensors**: ±5C (Internal measurement).

| Slot Number | A6 | A5 | A4 | A3 | A2/GA2* | A1/GA1* | A0/GA0* | Hardware Address | IPMB Address |
|---|---|---|---|---|---|---|---|---|---|
| Slot0 | 0 | 1 | 0 | 0 | 0 / U | 0 / U | 0 / U | 20 | 40 |
| Slot1 | 0 | 1 | 0 | 0 | 0 / U | 0 / U | 1 / G | 21 | 42 |
| Slot2 | 0 | 1 | 0 | 0 | 0 / U | 1 / G | 0 / U | 22 | 44 |
| Slot3 | 0 | 1 | 0 | 0 | 0 / U | 1 / G | 1 / G | 23 | 46 |
| Slot4 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 24 | 48 |
| Slot5 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 25 | 4A |
| Slot6 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 26 | 4C |
| Slot7 | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 27 | 4E |

**Table 3.7.2-1 Address Space**

***Note: A0÷A6 represent Firmware address and GAx represent the physical Geographical Address.***
**U = Unconnected; signal is pulled up on the unit and result as logic "0"**
**G = Biased to Ground on the Backplane; results in a logical "1"**

### 3.6.3 USB Programing

Firmware update can be done by accessing the USB connector on the front side of the unit.
Dedicated programing harness is required, please contact factory.
USB is 3.3V-5V level, 5V is Max Abs rating.

### 3.6.4 IPMC, 46.11 Tier2

The M4096 design to support both ELMA's ChM and IPMITOOL System Interface.
Adjustments can be made to support custom ChM configurations.

| Sensor ID | Sensor Type | Name | Function |
|---|---|---|---|
| 00 | F0h | FRU State Sensor | *ANSI/VITA 46.11-2022* ***10.2.1*** |
| 01 | F1h | System IPMB Link Sensor | *ANSI/VITA 46.11-2022* ***10.2.2*** |
| 02 | F2h | FRU Health Sensor | Asserted when output, input, or Vin is out of normal range per *Table 3.7.2.1-4* |
| 03 | 02h | FRU Voltage Sensor | Asserted when output voltage is out of normal range per *Table 3.7.2.1-4* |
| 04 | F3h | FRU Temperature Sensor | Asserted when unit internal temperature is out of normal range based on which threshold it has passed per *Table 3.7.2.1-4* |
| 05 | F4h | Payload Test Results Sensor | Self-test on IPMC to determine correct operation. *ANSI/VITA 46.11-2022* ***10.2.6*** |
| 06 | F5h | Payload Test Status Sensor | Sensor indicates whether payload test is in progress. *ANSI/VITA 46.11-2022* ***10.2.7*** |
| 07 | 02h | VS1 Voltage | VS1 Output Voltage |
| 08 | 03h | VS1 Current | VS1 Output Current |
| 09 | 02h | VS2 Voltage | VS2 Output Voltage |
| 10 | 03h | VS2 Current | VS2 Output Current |
| 11 | 01h | Analog Temperature | Internal temperature of unit located near IPMC |

**Table 3.6.2.1-1. Sensor Allocation**

| IPMITOOL Command |
|---|
| SDR List |
| Sensor List |
| Fru Print |
| SEL List |
| SEL Clear |

**Table 3.7.2.1-2. Supported *IPMITOOL* Commands**

| IPMI Command | NetFn | Group ID | CMD |
|---|---|---|---|
| Get Device ID | APP | N/A | 01h |
| Get Self-Test Results | APP | N/A | 04h |
| Get FRU Inventory Area Info | Storage | N/A | 10h |
| Read FRU Data | Storage | N/A | 11h |
| Set Event Receiver | S/E | N/A | 00h |
| Get Event Receiver | S/E | N/A | 01h |
| Get Device SDR info | S/E | N/A | 20h |
| Get Device SDR | S/E | N/A | 21h |
| Reserve Device SDR Repository | S/E | N/A | 22h |
| Get Sensor Reading | S/E | N/A | 2Dh |
| Get VSO Capabilities | Group Extension | VSO (03h) | 00h |
| Set IPMB State | Group Extension | VSO (03h) | 09h |
| Get Device Locator Record ID | Group Extension | VSO (03h) | 0Dh |
| Fru Control Capabilities | Group Extension | VSO (03h) | 1Eh |
| Get FRU Address Info | Group Extension | VSO (03h) | 40h |

**Table 3.7.2.1-3. Supported *RAW IPMI* Commands**

| Sensor Name | Parameter | Upper Non-Recoverable Threshold | Upper Critical Threshold | Upper Non-Critical Threshold | Lower Non-Critical Threshold | Lower Critical Threshold | Lower Non-Recoverable Threshold |
|---|---|---|---|---|---|---|---|
| VS1 12V | Voltage | 13V | 12.8V | 12.6V | 11.6V | 11.4V | 11.2V |
| | Current | | | | | | |
| 3.3VAux | Voltage | 4.2V | 4.0V | 3.8V | 3V | 2.8V | 2.6V |
| | Current | 24A | 22A | 20A | | | |
| Temperature | Temperature | 115°C | 110°C | 105°C | -55°C | -60°C | -60°C |
| Vin | Voltage | 340V | 290V | 280V | 250V | 240V | 190V |

**Table 3.7.2.1-4. Sensors Thresholds**

***Note: Threshold levels can be updated by request.***

### 3.6.5 Advanced I²C Communication

This communication protocol serves as an option when 46.11 ChM is not used. A more basic I2C protocol is optional when system can't support 46.11 IPMC.

### 3.6.6 DO254 Supportable version

For systems which would like to certify DO-254 and avoid DO-178, a more simplified communication approach is available. Please contact factory for additional information.

## 3.7 Pinout

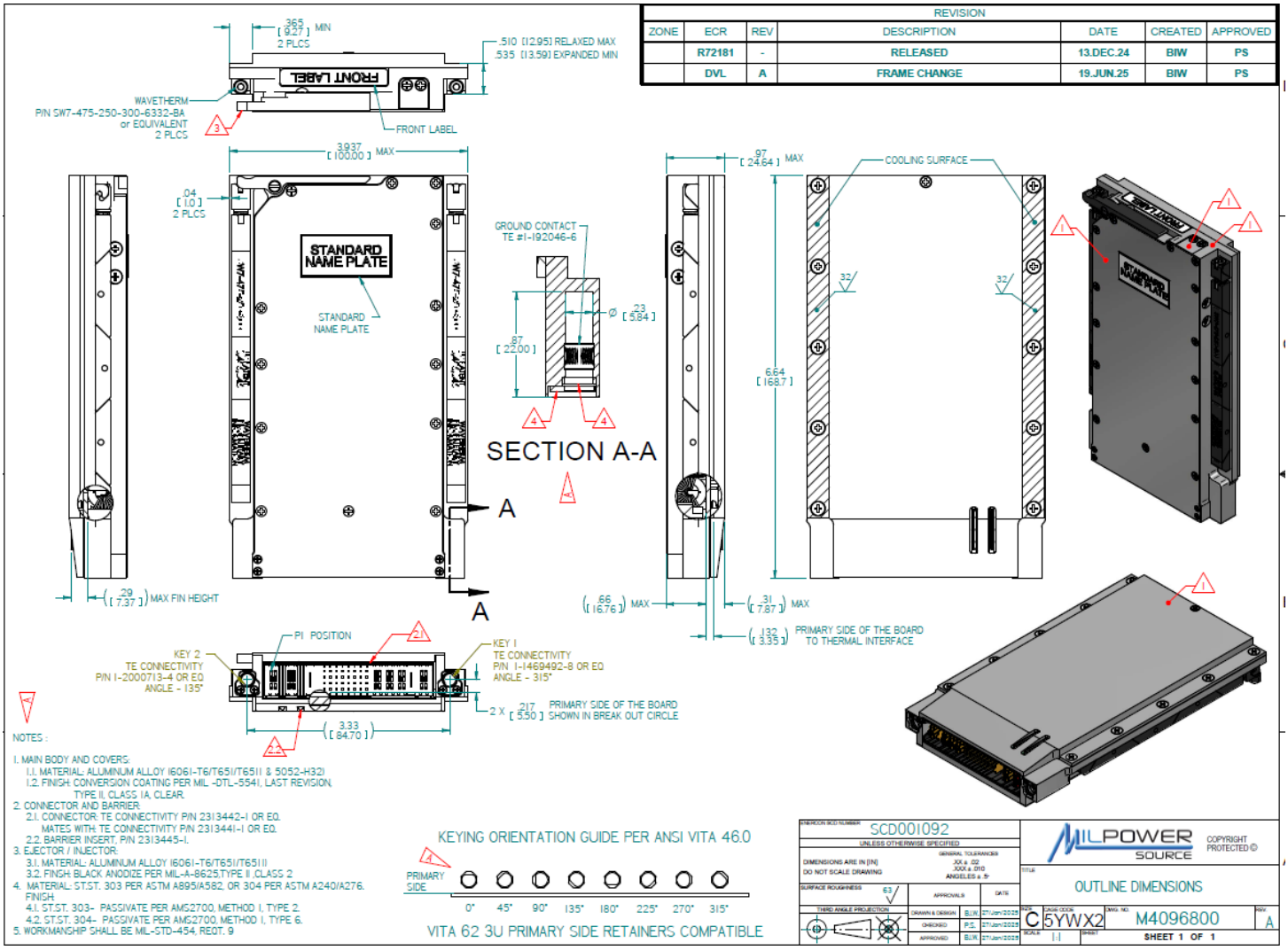
### 3.7.1 P1 Connector

| *Pin Number* | *Pin Name (12V Only)* | *Function* |
|---|---|---|
| P1 | -DC_IN/ACN | 270V Return |
| P2 | +DC_IN/ACL | 270V |
| LP1 | CHASSIS | CHASSIS |
| P3 | +12VDC (VS1) | 12V Output |
| P4 | POWER_RETURN | Output Return |
| P5 | POWER_RETURN | Output Return |
| LP2 | 3.3V_AUX | 3.3V Output |
| P6 | +12VDC (VS1) | 12V Output |
| A8 | SENSE, +12VDC | 12V Sense |
| B8 | SENSE, 3.3V_AUX | 3.3V Sense |
| C8 | SENSE, +12VDC | 12V Sense |
| D8 | SENSE_RETURN | Sense Return |
| A7 | SHARE_1 | 12V Current Share |
| B7 | SHARE_2 | 3.3V Current Share |
| C7 | SHARE_3 | 12V ACS |
| D7 | SIGNAL RETURN | Signal Return |
| A6 | SM2 | $I^2C$ SCL B |
| B6 | SM3 | $I^2C$ SDA B |
| C6 | N Reserved C. | D.N.C. |
| D6 | SYSRESET* | SYSRESET* |
| A5 | GA0* | GA0* |
| B5 | GA1* | GA1* |
| C5 | SM0 | $I^2C$ SCL A |
| D5 | SM1 | $I^2C$ SDA A |
| A4 | Reserved | D.N.C. |
| B4 | Reserved | D.N.C. |
| C4 | Reserved | D.N.C. |
| D4 | Reserved | D.N.C. |
| A3 | SYNC_IN (UD0) | External Sync Input |
| B3 | Reserved | D.N.C. |
| C3 | NED | D.N.C. |
| D3 | NED RETURN | D.N.C. |
| A2 | VBAT | D.N.C. |
| B2 | FAIL* | FAIL* |
| C2 | INHIBIT* | INHIBIT* |
| D2 | ENABLE* | ENABLE* |
| A1 | SYNC_OUT (UD1) | External Sync Output |
| B1 | NVMRO (UD2) | NVMRO |
| C1 | GA2* (UD3) | GA2 |
| D1 | UD4 | 3.3V ACS |

### 3.7.2 Programming Connector

Programming connectors are available. Please contact factory for information.

## 3.8 Mechanical SCD



## Appendix A – VITA 47 Compliance (For full compliance please contact Factory)

### A.1 Environmental VITA 47 CCW7 NT4 V3 OS2 C4 AV2 SF1/2/3 CS5 M3

### A.2 Design

### A.3 Safety

### A.4 Quality

## Appendix B – Restricted materials (For full compliance please contact Factory).